

## REMARKS

Claims 1, 2, 4, 7, 10, 11, 16, 19 and 20 have been amended, and claims 6, 8, 9, 12, 13, 17 and 18 have been canceled by this Response. Claims 1-5, 7, 10, 11, 14-16, 19 and 20 remain pending in the application for consideration. Applicants respectfully request further examination of the application, as amended, in view of the following remarks.

### *Rejection of Claims 1, 3-10, 12-14, 17, 18 and 20 Under 35 U.S.C. § 102(e) -- Althaus*

Claims 1, 3-10, 12-14, 17, 18 and 20 stand rejected under 35 U.S.C. § 102(e) as anticipated by *Althaus* (U.S. Patent No. 6,731,882 to Althaus, et al.). Applicants have amended independent claims 1 and 10, from which the remaining claims under this rejection depend, to emphasize various aspects of the invention, but otherwise respectfully traverse this rejection.

With regard to claims 1 and 10 (and, by dependency, the remaining claims under this rejection), there are various aspects of the invention as claimed that are not disclosed in *Althaus*. For example, *Althaus* does not disclose a sub-mount wafer portion or a cap wafer portion. Rather, the element labeled with reference numeral “1” in *Althaus* that the Examiner contends is a sub-mount is a leadframe. A leadframe is made of metal and is not made of semiconductor wafer material.

Significant features of Applicants' invention as it is set forth in these claims include that a sub-mount wafer portion and a cap wafer portion have mating surfaces that are bonded together to form a package that encloses a die. The die contains a laser and is mounted on a first surface of the sub-mount wafer portion, within a cavity in the cap wafer portion. A cavity wall defines a reflector, which reflects light emitted by the laser in a direction toward the first surface of the sub-mount wafer portion. The light passes through the sub-mount wafer portion and emerges in the same direction, from the opposing (second) surface of the sub-mount wafer portion. Such a device is shown in, for example, FIGS. 1-2 of the present application. In some embodiments this device can exist at a wafer level (i.e., in multiple instances across an assembly comprising a sub-mount wafer and cap wafer) or, in other embodiments, can exist independently as a single device that has been cut from such a wafer assembly.

In contrast, *Althaus* discloses a structure in which a die (11) is mounted on a leadframe, and a laser on the die emits light into a deflection prism, which deflects the light in a direction toward the leadframe. The light passes through an opening in the leadframe. Optical elements mounted in a mirror mount structure (8) below the leadframe reflect the light in a U-shaped path, first in a direction parallel to the plane of the leadframe and then back through another opening in the leadframe toward a detector. Not only does *Althaus* not disclose any wafer portions other than the die itself, but *Althaus* does not disclose a cavity having a reflective surface in any such wafer portion or that reflected light passes through the (sub-mount) wafer portion. Rather, in *Althaus* the reflected light passes through an opening in a leadframe. The leadframe itself is opaque metal and does not have any portion through which light can pass. Furthermore, the reflected light in *Althaus* does not emerge from a second surface in the same direction in which it impinged upon an opposing first surface. Indeed, if the mirror mount structure (8) is interpreted as part of the sub-mount, as the Examiner appears to interpret it, light does not emerge at all from a second surface of the mirror mount structure (8) but rather is reflected in a U-shaped path within the mirror mount structure (8). For at least the foregoing reasons, Applicants respectfully submit that claims 1 and 10, and by dependency, claims 3-9, 12-14, 17, 18 and 20, are not anticipated by *Althaus*.

***Rejection of Claims 9 and 13 Under 35 U.S.C. § 103(a) – Althaus and Kilian***

Claims 9 and 13 stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Althaus* in view of *Kilian* (U.S. Patent Application Publication No. 2004/0190836 of *Kilian*). Claims 9 and 13 have been canceled without prejudice. Accordingly, Applicants respectfully submit that this rejection is moot.

***Rejection of Claims 2, 11 and 19 Under 35 U.S.C. § 103(a) – Althaus and Freeman***

Claims 2, 11 and 19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Althaus* in view of *Freeman et al.* (U.S. Patent No. 5,195,156 to *Freeman, et al.*). Claims 1 and 10, from which claims 2, 11 and 19 depend, have been amended as discussed above, but Applicants otherwise traverse this rejection.

Claims 2, 11 and 19 relate to an alignment post that is attached to the sub-mount wafer portion where the optical signal emerges from the second surface of the sub-mount wafer portion. *Freeman et al.* discloses an optical connector assembly that includes a

cylindrical “member 200” that the Examiner characterizes as an alignment post. As described in *Freeman et al.*, the member (200) aids coupling an optical fiber to a printed circuit board on which a laser diode is mounted. Applicants respectfully submit that coupling an optical fiber to a printed circuit board is not similar to coupling an optical fiber to a semiconductor die or other wafer portion. There is nothing about using a cylindrical member (200) to couple an optical fiber to a printed circuit board that would have motivated a person of ordinary skill in the art to have attached a post to a structure comprising two wafer portions bonded together, so that light emitted through a surface of one of the wafers could be coupled into the fiber.

It should also be recognized that in Applicants’ invention as it is set forth in the claims from which claims 2, 11 and 19 depend, the light passes “through” the sub-mount wafer portion. That is, the sub-mount wafer portion has a portion that is transparent to the light or otherwise allows light to pass through it. Absent the alignment post, there is nothing on the second surface of the sub-mount wafer portion that indicates the point from which the light would emerge. To solve this problem, Applicants’ invention can include an alignment post that not only transmits the light emerging from the second surface into an optical fiber but also serves as an index or alignment point on the second surface to facilitate attachment of a fiber. More specifically, as described in Applicants’ specification, a sleeve can be used to attach a fiber-retaining ferrule to the alignment post, thereby aligning the fiber with the point on the second surface of the sub-mount wafer portion from which the light emerges. Nothing in *Freeman et al.* discloses or suggests such a structure or method.

Accordingly, Applicants respectfully submit that the invention as it is set forth in claims 2, 11 and 19 would not have been obvious to a person of ordinary skill in the art in view of only the combined teachings of *Althaus* and *Freeman et al.*

***Rejection of Claims 15 and 16 Under 35 U.S.C. § 103(a) – Althaus and Mizutani et al.***

Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Althaus* in view of *Mizutani et al.* (U.S. Patent No. 5,822,352 to Mizutani, et al.). Claim 10, from which claims 15 and 16 depend, has been amended as discussed above, but Applicants otherwise traverse this rejection.

Although the Examiner observes that, as exemplified by *Mizutani et al.*, it is known in the art to form semiconductor lasers on wafers by crystal growth methods “and further to cut

the separately grown components on the wafers into separate parts,” Applicants respectfully submit that this knowledge alone would not have motivated a person of ordinary skill in the art to have formed a structure comprising a sub-mount wafer portion and cap wafer portion bonded together and then cut the resulting structures into separate packages.

The above-referenced aspect of Applicants’ invention to which claims 15 and 16 relates can be referred to as wafer-level packaging. Wafer-level packaging can be contrasted with the die-level packaging of an integrated circuit die that is most commonly performed after the dice are separated from one another, i.e., after the wafer is cut or separated into portions known as dice. In Applicants’ invention as it is set forth in these claims, some of the packaging aspects that are conventionally included at die level are included in Applicants’ invention at the wafer level. Specifically, the combination of the cap wafer portion and sub-mount wafer portion defines a package that encloses the laser and other elements in a manner analogous to enclosing a conventional die within a package. In the present invention, the cap wafer portion serves as part of the package as well as a reflector. Packaging the structure in the manner set forth in claim 16 can obviate some conventional packaging steps.

*Mizutani et al.* does not even relate to wafer-level packaging. Rather, *Mizutani et al.* discloses little more than is relevant to the claimed invention than the conventional steps involved in manufacturing semiconductor chips whereby multiple instances of the chip circuitry are formed across a wafer, and the wafer is subsequently cut into individual dice or chips, each containing the circuitry. This knowledge would not, either alone or in combination with the teachings of *Althaus*, have motivated a person of ordinary skill in the art to have considered the processes set forth in claims 15 and 16. Accordingly, Applicants respectfully submit that claims 15 and 16 would not have been obvious to a person of ordinary skill in the art in view of *Mizutani et al.* and *Althaus*.

## CONCLUSION

In view of the foregoing, Applicants respectfully submit that all grounds of rejection have been successfully traversed and/or overcome and that that application is in condition for allowance. Should the Examiner have any comment regarding Applicants' response or believe that a teleconference would expedite examination of the pending claims, Applicants respectfully request that the Examiner telephone Applicants' undersigned attorney.

Respectfully submitted,

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